REMARKS

This Response is submitted in response to the Final Office Action of December 15, 2004 (hereinafter "the Office Action"). Claims 1, 3, 4, 17, and 18 remain pending and stand rejected under 35 U.S.C. §102(b). Applicant notes with appreciation the withdrawal of rejections under 35 U.S.C. § 112, second paragraph.

In the following remarks, all references to the claims, except as noted, will be made with reference to the claim list above beginning on page 2. All references to "the Office Action," except as noted, will be referencing the most recent Office Action dated December 15, 2004. Line numbers in the Office Action, except as noted, will count every printed line, except the page header, but including section headings. If there is any confusion or questions regarding any aspect of this Amendment, the Examiner is invited to contact the undersigned.

Claim Rejections -- 35 U.S.C. § 102(b)

Claims 1, 3, 4, 17, and 18 stand finally rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 4,864,494 issued to Kobus, Jr. (hereinafter, "Kobus"). Applicant traverses because Kobus does not disclose each and every element of the invention as set forth in the claims.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See MPEP 2131. Therefore, the presence of a single claim element not disclosed by the prior art reference cited in the rejection is sufficient to overcome an anticipation rejection under 35 U.S.C. § 102. There are many differences between the claimed invention and the Kobus; the claim elements mentioned in the following discussion are presented as examples only of the many differences.

Claim 1 sets forth a central processor chip having several components. In addition to processor circuitry (claim 1, line 5) and RAM (claim 1, line 7), claim 1 sets forth "a programmable error correcting circuit on said chip" (claim 1, line 6).

In contrast, Kobus discloses a security device for a computer comprising a key device that connects to a computer or other device using a serial (RS-232) connection. The Office Action suggests that the microprocessor on the key device reads on the processor chip set forth in claim 1 (page 3, lines 1-5). However, the Office Action fails to point out how or what part of Kobus reads on an error correcting circuit. Instead, the Office Action summarizes the operation of Kobus (Office Action, page 3, lines 6-18) and then conclusively states that the reference meets the claim limitations (Office Action, page 3, lines 18 to page 4, line 6).

Applicant respectfully submits that there is nothing, even in the summary of Kobus provided in page 3 of the Office Action, which reads on an error correcting circuit. In fact, the Office Action never even points to ***any*** error correcting function of Kobus. This is because Kobus *has no error correcting function.* The software that runs on the computer disclosed by Kobus includes statements designed to cause an error and end the program, but the error is *never corrected.* Rather, Kobus will execute statements designed to cause an error only if the security message received from the security key is invalid. See Figure 3, function block 63 and associated text at col. 17, lines 54-61. Thus, the error-causing code is never corrected; it is simply never executed when the security code is valid.

Kobus teaches a key device that includes a microprocessor and ROM-encoded program and data variables (col. 5, lines 1-2 and 10-12). The key device of Kobus communicates with the computer in a complex handshaking protocol to identify the sub-key (which corresponds with specific software) and pass a double-encrypted security key, as illustrated in Figure 3, of Kobus. There is no mention that the key device in any way performs any error correcting function or has error correcting circuitry on the chip. The key does not correct errors, it merely contains an encrypted security message used by the main software on the computer to which the key device is connected to null errors. The software encoded on the ROM does not contain errors and no encryption or error correction of this code is necessary since, "investigation . . . of the ROM encoded program and data variables is not possible" (col. 5, lines 10-12; see also col. 19, lines 7-12).

Even if the encryption key provided by the key device of Kobus were used to correct errors in the computer software, a proposition with which Applicant strenuously disagrees, it would not be fair to suggest that the "programmable error correcting circuitry" may be so broadly interpreted as to read on the key device of Kobus. Applicant notes that, during examination, the Examiner is obliged to give claim elements the broadest reasonable

interpretation to claim elements, and this interpretation must be consistent with the interpretation that those skilled in the art would reach. See MPEP 2111. The phrase, "error correcting circuit," which is on the processor chip itself, as set forth in line 6 of claim 1, would have been understood to be limited to a specialized error correcting circuit, not a the processor as a whole. Furthermore, the phrase, "error correcting circuit" would not have been interpreted to read on a key device that provides a security code to a software program to prevent an erroneous statement from executing. Even if the security code provided by the key device was used to correct an error--again, a proposition with which Applicant would disagree--the *key device* is not correcting the error and therefore no circuit in the key device is "error correcting." Such an interpretation would be inconsistent with the plain meaning, the ordinary and customary meaning that persons skilled in the art would attribute to it, and it would make no sense in the context of the claim as a whole, and would be inconsistent with the specification.

Therefore, there is no disclosure by Kobus of a key device having microprocessor with an on-chip programmable error correcting circuit. Since Claim 1 sets forth, "a programmable error correction circuit on said chip," Applicant respectfully submits that claim 1 is not anticipated by Kobus. Furthermore, investigation of other prior art of record reveals that claim 1 is not anticipated or made obvious by any prior art of record. Accordingly, Applicant respectfully submits that claim 1 is allowable, and further, that claims 3, 4, and 13, which depend from claim 1, are also allowable for at least the same reasons as claim 1. Furthermore, claim 17 sets forth, "a programmable error correcting circuit on said chip" (line 6) and claim 18 sets forth, inter alia, "on said chip, correcting said instructions using said error correction control information" (lines 7-8). Accordingly, Applicant respectfully submits that claims 17 and 18, which include limitations similar to that of claim 1 discussed above, should also be allowed for the same reasons as claim 1, also discussed above.

Claim 1 furthermore sets forth that the error correcting circuit (established above as being located *on the chip*) "receives said error correcting information and processor instructions containing errors" (lines 9-10). The Office Action has identified the key device containing the processor chip having error correction circuitry above. However, the key device *never* receives processor instructions containing errors. Processor instructions for the computer is never sent to the key device, and the software executed by the microprocessor on the key device does not contain errors and is not encrypted. Kobus is very clear that only security messages containing specific codes, keys, and other data is transmitted to the key

device, and no mention is made of processor instructions being sent to the key device from the computer. Furthermore, Kobus states that the key device includes a chip-based microprocessor with ROM memory (col. 5, lines 2-3), that the ROM contains the software that drives the microprocessor (col. 5, lines 9-12), and that the ROM is secure and cannot be accessed "by the outside world" (col. 5, lines 9-12; col. 19, lines 7-12) which therefore teaches away from encrypting the ROM software or encoding it with errors.

Is the Office interpreting the term, "processor instructions" so broadly as to encompass encrypted and non-encrypted security messages passed back and forth between the key device and the computer? If so, this is an unfair interpretation of the term, "processor instructions" which has plain meaning in the art as being information usable directly by a processor that causes the processor to perform designated operations. Furthermore, the specification distinguishes between "data" and "instructions" – see page 22, lines 27-32. The Office is constrained to interpret words to the broadest *reasonable* interpretation, and it is unreasonable to suggest that "instructions" would have been understood by persons of ordinary skill in the art to mean data passed back and forth between the key device and computer of Kobus. Furthermore, the specification's definition of "instructions" as being distinct from "data" (page 22, lines 27-32) constrains the Office's interpretation thereof.

Since Kobus does not disclose a programmable error correcting circuit that receives error correcting information and processor instructions containing errors, Applicant respectfully submits that Kobus does not anticipate claim 1. Furthermore, claims 3, 4, and 3 depend from claim 1 and are not anticipated by Kobus for at least the same reasons as claim 1. Furthermore, claims 17 and 18 set forth similar limitations in lines 10-12 and 7-8, respectively, and are therefore also not anticipated by Kobus. Furthermore, none of the references of record, either singly or in combination teach or suggest this element. Therefore, Applicant respectfully submits that pending claims 1, 3, 4, 13, 17, and 18 are allowable and a notice of allowability is earnestly requested.

In addition to the claim elements set forth above, independent claims 1, 17, and 18 set forth additional limitations which distinguish the invention from the prior art. Furthermore, claims 3, 4, and 13 depend from claim 1 and further define and distinguish the invention from the prior art, thereby giving rise to separate reasons for allowability.

For all the reasons noted above and others, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present amendment, the Examiner is kindly requested to contact the undersigned at (408) 774-6933. If any other fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (SUNMP210). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
MARTINE & PENILLA, LLP

Leonard Heyman, Esq.
Reg. No. 40, 418

710 Lakeway Drive, Suite 200
Sunnyvale, CA 94085
Telephone: (408) 749-6900
Facsimile: (408) 749-6901
Customer Number 32291